CLAIMS:

1. Digital amplifier, comprising: a half bridge system with switches; a switching-timing correction circuit to which an input signal and an output signal of the switches in applied; wherein the switching-timing correction circuit corrects switching timing errors of the switches on the basis of pulse-timing errors of the input signal of the switches and the output signal of the switches.

2. The digital amplifier of claim 1, wherein the switching-timing correction circuit corrects switching timing errors of the switches by delaying at least one of a rising edge and a falling edge of a pulse of the input signal.

3. The digital amplifier of claim 1, wherein the switching-timing correction circuit comprises: a pulse edge delay detector for detecting an on/off-difference between an on-delay of a pulse supplied to the switches and an off-delay of the pulse response output by the switches; and an error signal generator for generating an error signal on the basis of the on/off-difference; wherein the error signal corresponds to the pulse-timing errors between the input signal of the switches and the output signal of the switches; and wherein the switching-timing correction circuit corrects switching timing errors of the switches on the basis of the error signal.

4. The digital amplifier of claim 3, wherein the error signal is generated from one switching cycle and influences switching edges of a subsequent switching cycle.

5. The digital amplifier of claim 3, wherein the error signal is averaged over a predetermined number of switching cycles by means of an averaging circuit to reduce a sub-harmonic injection.

6. The digital amplifier of claim 3, wherein the error signal is generated by means of an integration capacitor; and wherein the digital amplifier is a class D amplifier.

7. Switching-timing corrector for correcting switching timing errors of switches of a bridge of a digital amplifier, the switching-timing corrector comprising: a pulse edge delay detector for detecting an on/off-difference between an on-delay of a pulse supplied to the switches and an off-delay of the pulse response output by the switches; an error signal generator for generating an error signal on the basis of the on/off-difference; an input pulse delay circuit for correcting switching timing errors of the switches by delaying at least one of a rising edge and a falling edge of a pulse of the input signal on the basis of the error signal.

8. The switching-timing corrector of claim 7, wherein the error signal is generated from one switching cycle and influences switching edges of a subsequent switching cycle.

9. The switching-timing corrector of claim 7, wherein the error signal is averaged over a predetermined number of switching cycles by means of an averaging circuit to reduce a sub-harmonic injection.

10. The switching-timing corrector of claim 7, wherein the error signal is generated by means of an integration capacitor; and wherein the switching-timing corrector is adapted for connection to a class D amplifier.

11. Method of correcting pulse-timing errors of switches of a bridge of a digital amplifier, the method comprising the steps of: detecting rising and falling pulse edges of an input and an output signal of the switches; generating an error signal corresponding to pulse edge delays between the rising and falling pulse edges of the input and the output signal; and correcting switching timing errors of the switches on

the basis of the error signal.

12. The method of claim 11, wherein the switching timing errors of the switches are corrected by delaying at least one of the rising edge and the falling edge of a pulse of the input signal.

13. The method of claim 11, wherein the error signal is generated from one switching cycle and influences switching edges of a subsequent switching cycle.

14. The method of claim 11, wherein the error signal is averaged over a predetermined number of switching cycles by means of an averaging circuit to reduce a sub-harmonic injection.